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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

Application Number: 09/961,024  
Filing Date: September 21, 2001  
Appellant(s): MEARS ET AL.

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Robert E. Mates  
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed June 15, 2006 appealing from the Office action mailed January 12, 2006.

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**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

6,333,938	Baker	12-2001
6,226,338	Earnest	5-2001

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6,122,680	Holm et al.	9-2000
6,816,935	Gulick	11-2004
5,396,635	Fung	3-1995
5,317,749	Dahlen	5-1994
5,088,024	Vernon et al.	2-1992
6,697,904	Bennett	2-2004

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-14, 16-18, 28-31, 33-34, 36-44 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker(6,333,938), in view of Earnest(6,226,338).

Regarding claim 1, Baker discloses a communications interface, comprising: a bus interface(Figure 1, 20) coupleable to an internal bus(Figure 1, 24), a plurality of transmit channels coupled to the bus interface(DMA channels; Column 5, Lines 45-53); a transmit control block coupled to the plurality of transmit channels(Figure 2, 72 and 90 combined); a plurality of outbound links coupled to a plurality of outputs of the transmit control block; a plurality of receive channels coupled to the bus interface(DMA channels; Column 5, Lines 45-53); and a receive control block(Figure 2, 72 and 90 combined) coupled to the plurality of receive channels; and a plurality of inbound links coupled to a plurality of inputs of the receive control block, the inbound links and the outbound links to couple the bus interface to a further bus interface(Figure 1, 18) and a start message channel coupled to the receive control block and adapted to send a start message to the source when the receive FIFO reaches a start threshold value(Column 19, Lines 7-15).

Baker does not specifically disclose a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO reaches a stop threshold value. However, Earnest discloses a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO reaches a stop threshold value (Column 11, Lines 40-45). Therefore, it would have been obvious to include the stop message channel, as disclosed by Earnest, in the system of Baker, since this would prevent the writing of data in FIFO that has no more room for data.

Regarding claim 2, Baker discloses a communications interface, further comprising a direct memory access controller (Figure 2, 72) coupled to the bus interface.

Regarding claim 3, Baker discloses a communications interface, wherein the bus interface comprises a plurality of transmit control registers and a plurality of receive control registers (Figure 2, 88).

Regarding claim 4, Baker discloses a communications interface, wherein the plurality of transmit control registers comprises a transmit first in first out (FIFO) register associated with each transmit channel (Figure 2, 82, 84) and a channel status register associated with each transmit channel (Figure 2, 88).

Regarding claim 5, Baker discloses a communications interface, wherein the plurality of receive control registers comprises a receive FIFO register coupled to each receive channel (Figure 2, 80) and a channel status register associated with each receive channel (Figure 2, 88).

Regarding claim 6, Baker discloses a communications interface, wherein each of the plurality of transmit channels and each of the plurality of receive channels comprises a first in first out (FIFO) memory device (Figure 2, 80, 82, 84).

Regarding claim 7, Baker does not specifically disclose a power management unit coupled to each of the plurality of transmit channels and receive channels. However, Official Notice is being taken that advantages of power management are well known in the art and it would have been obvious to include a power management unit in the system of Baker since this would allow power to be saved during periods of inactivity(The common knowledge or well-known in the art statement was taken to be admitted prior art because applicant either failed to traverse the examiner's assertion of official notice (see MPEP 2144.03 (C))).

Regarding claim 8, Baker discloses a communications interface, wherein the transmit control block comprises a channel arbiter adapted to select a next one of the plurality of transmit channels to be activated(Figure 12, 340).

Regarding claim 9, Baker discloses a communications interface, wherein the transmit control block comprises a link controller adapted to transmit data from a selected transmit channel across a selected link.(Figure 2, 90).

Regarding claim 10, Baker discloses a communications interface, wherein the receive control block comprises a state machine adapted to store a current active channel number, a number of bits in a current byte being transferred and to write each byte to a selected one of the plurality of receive channels(Figure 12, 352; Column 13, Lines 12-14).

Regarding claim 11, Baker discloses a communications interface, wherein the plurality of transmit channels comprises: at least one channel adapted to send a clock signal(Figure 26b, clkA); at least one channel adapted to send a strobe signal(Figure 12, 356); at least one channel adapted to send a wait signal(Column 26, Lines 40-41); and at least one channel adapted to send data(Column 26, Lines 66-67).

Regarding claim 12, Baker discloses a communications interface, wherein the plurality of receive channels comprises: at least one channel adapted to send a clock signal(Figure 26b,

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clkB); at least one channel adapted to send a strobe signal(Figure 12, 356); at least one channel adapted to send a wait signal(Column 25, Lines 20-23); and at least one channel adapted to send data(Column 25, Lines 28-29).

Regarding claim 13, Baker discloses a communications interface, wherein at least one of the plurality of transmit channels and the plurality of receive channels comprise a virtual general purpose input/output channel(Column 7, Lines 42-43).

Regarding claim 14, Baker discloses a communications interface, further comprising: a start threshold register adapted to set a start threshold value to cause a start message to be sent to a source when the receive FIFO can receive additional data(Column 19, Lines 7-15) and Earnest discloses a stop threshold register adapted to set a threshold value to cause a stop message to be sent to a source when a receive FIFO is full(Column 11, Lines 40-45).

Regarding claim 16, Baker does discloses at least one of a direct flow control mode and a message flow control to control a flow of data across the communications interface(Column 19, Lines 7-15).

Regarding claim 17, Baker discloses a communications interface, wherein the transmit control block comprises: a multiplexer coupled to the plurality of transmit channels; a parallel in serial out converter (PISO)(Column 6 Lines 20-22) coupled to the multiplexer; and a control circuit coupled to the multiplexer and the PISO and adapted to select one of the plurality of transmit channels to transmit data(Fig 12, 344).

Regarding claim 18, Baker discloses a communications interface, wherein the receive control block comprises: a demultiplexer coupled to the plurality of receive channels; a serial in parallel out converter (SIPO)(Column 6 Lines 20-22); and a control circuit coupled to the demultiplexer and adapted to select one of the plurality of receive channels to receive data((Fig 12, 344).

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Regarding claim 28, Baker discloses a method of transmitting data between semiconductor chips, comprising writing data into at least one of a plurality of transmit FIFOs(Figure 2, 82, 84); selecting one of the plurality of transmit FIFOs that contains data to be transmitted and that is not in a wait state(Column 14, Lines 20-28; Column 18, Lines 58-60) and sending a start message when the corresponding one of the receive FIFOs can receive data(Column 19, Lines 7-15).

Baker does not disclose and transmitting the data to a corresponding one of the plurality of receive FIFOs that has not exceeded a threshold value and sending a stop message if the corresponding one of the receive FIFOs cannot receive data. However, Earnest discloses and transmitting the data to a corresponding one of the plurality of receive FIFOs that has not exceeded a threshold value and sending a stop message if the corresponding one of the receive FIFOs cannot receive data(Column 11, Lines 40-45). Therefore, it would have been obvious the teachings of Earnest, with that of Baker, since this would prevent the writing of data in FIFO that has no more room for data.

Regarding claim 29, Baker discloses a method, further comprising: sending a wait signal to a transmit control block if the corresponding one of the receive FIFOs cannot receive data; and removing the wait signal when the corresponding one of the receive FIFOs can receive data(Column 26, Lines 40-41).

Regarding claim 30, Baker discloses a method, further comprising selecting another one of the plurality of transmit FIFOs to send data to another corresponding one of the plurality of receive FIFOs while the corresponding one of the receive FIFOs cannot receive data(Column 14, Lines 20-28; Column 17, Lines 1-15).

Regarding claim 31, Baker discloses a method, further comprising: sending a strobe signal to initiate a transmission of data(Figure 12, 356); sending a selected channel number



over which the data is to be transmitted(Column 14, Lines 20-28); and sending an end of message signal after the data has been transmitted(Column 25, Lines 62-64).

Regarding claim 33, Baker discloses a method, further comprising: selecting one of the plurality of transmit FIFOs and the corresponding one of the plurality of receive FIFOs by a predetermined algorithm(Figure 13).

Regarding claim 34, Baker does not disclose the predetermined algorithm is round-robin. However, the round-robin algorithm is a well-known arbitration scheme and therefore could be substituted for the arbitration scheme in Baker's system for fairness to all channels.

Regarding claim 36, Baker discloses a method of forming a communications interface, comprising: forming a bus interface(Figure 1, 20), forming a plurality of transmit channels coupled to the bus interface(DMA channels; Column 5, Lines 45-53); forming a transmit control block coupled to the plurality of transmit channels(Figure 2, 72 and 90 combined); forming a plurality of outbound links coupled to a plurality of outputs of the transmit control block; forming a plurality of receive channels coupled to the bus interface(DMA channels; Column 5, Lines 45-53); forming a receive control block(Figure 2, 72 and 90 combined) coupled to the plurality of receive channels; forming a plurality of inbound links coupled to a plurality of inputs of the receive control block, the inbound links and the outbound links to couple the bus interface to a further bus interface(Figure 1, 18) and forming a start message channel coupled to the receive control block and adapted to send a start message to the source when the receive FIFO reaches a start threshold value(Column 19, Lines 7-15).

Baker does not specifically disclose forming a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO reaches a stop threshold value. However, Earnest discloses forming a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a

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receive FIFO reaches a stop threshold value(Column 11, Lines 40-45). Therefore, it would have been obvious to include the stop message channel, as disclosed by Earnest, in the system of Baker, since this would prevent the writing of data in FIFO that has no more room for data.

Regarding claim 37, Baker discloses a method, wherein forming the bus interface comprises forming a plurality of transmit control registers and a plurality of receive control registers((Figure 2, 88).

Regarding claim 38, Baker discloses a method, wherein forming the transmit control block comprises: forming a channel arbiter adapted to determine a next one of the plurality of channels to be activated(Figure 12, 340); and forming a link controller adapted to transmit data from a selected transmit channel across a selected link(Figure 2, 90).

Regarding claim 39, Baker discloses a method, wherein forming the receive control block comprises forming a state machine adapted to store a currently active channel number, a number of bits in a current byte being transferred and to write each byte to a selected one of the plurality of receive channels(Figure 12, 352; Column 13, Lines 12-14).

Regarding claim 40, Baker discloses a method, wherein forming the plurality of transmit channels and forming the plurality of receive channels, each comprises: forming at least one channel adapted to send a clock signal(Figure 26b, clkA, clkB); forming at least one channel adapted to send a strobe signal(Column 12, 356); forming at least one channel adapted to send a wait signal(Column 26, Lines 40-41; Column 25, Lines 20-23); and forming at least one channel adapted to send data(Column 25, Lines 28-29; Column 26, Lines 66-67).

Regarding claim 41, Baker discloses a method, further comprising forming at least one virtual general purpose input/output channel(Column 7, Lines 42-43).

Regarding claim 42, Baker discloses a method, wherein forming the transmit control block comprises: forming a multiplexer coupled to the plurality of transmit channels; forming a

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parallel in serial out converter (PISO)(Column 6, Lines 20-22) coupled to the multiplexer; and forming a control circuit coupled to the multiplexer and to the PISO(Figure 12, 344).

Regarding claim 43, Baker discloses a method, wherein forming the receipt control block comprises: forming a demultiplexer coupled to the plurality of receive channels; forming a serial in parallel out converter (SIPO)(Column 6; Lines 20-22); forming a control circuit coupled to the demultiplexer and adapted to select one of the plurality of receive channels to receive data(Figure 12, 344).

Regarding claim 44, Baker discloses a method comprising: supplying a clock signal from a first terminal; supplying a strobe signal from a second terminal; providing an identification value corresponding to a selected channel register from data terminals when the strobe signal is active; providing data from the selected channel register at the data terminals when the strobe signal is inactive, the data changing in accordance with the clock signal; and providing a third terminal that receives a wait signal that keeps the data provided at the data terminals from changing(Figure 12, Column 17, Lines 34-50) and providing a start message channel coupled to the receive control block and adapted to send a start message to the source when the receive FIFO reaches a start threshold value(Column 19, Lines 7-15).

Baker does not specifically disclose providing a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO reaches a stop threshold value. However, Earnest discloses providing a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO reaches a stop threshold value(Column 11, Lines 40-45). Therefore, it would have been obvious to include the stop message channel, as disclosed by Earnest, in the system of Baker, since this would prevent the writing of data in FIFO that has no more room for data.

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Regarding claim 49, Baker discloses a communications interface, further comprising: a channel start threshold register to store the start threshold value to cause a start message to be sent to a source when the receive FIFO can receive additional data(Column 19, Lines 7-15) and Earnest discloses a stop threshold register adapted to set a threshold value to cause a stop message to be sent to a source when a receive FIFO is full(Column 11, Lines 40-45).

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baker, in view of Earnest, and in further view of Holm(6,122,680).

Baker and Earnest does not disclose a method, further comprising selecting an interface width from one of a serial width, a two-bit width and a nibble width. However, Holm discloses width of the data bus being any size(Column 8, Lines 31-32). Therefore it would have been obvious to use the teachings of Holm in the system of Baker and Earnest, to use a bus with varying width since this would increase compatibility.

#### **(10) Response to Argument**

In response to appellant's argument that there is no evidence of a suggestion or motivation to combine the references, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, data is stored in a FIFO during a data transfer. During the data transfer, the FIFO may become full if the data transfer requires more data than the size of the FIFO. IF additional data is transferred after the FIFO becomes full, the FIFO will become overrun with data and cause data corruption. Therefore, it would have been obvious to include the stop message channel, as disclosed by Earnest(Column 4, Lines 40-44) in the

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system of Baker, since this would prevent the writing of data in the FIFO that has no more room for additional data and therefore prevent buffer overrun, which is knowledge generally available to one of ordinary skill in the art. As further evidence, Bennett(6,697,904) discloses the data transfer being halted when the FIFO becomes full to prevent data corruption(Column 2, Lines 1-5).

In response to appellant's argument that there is no evidence of a reasonable expectation of success, Examiner notes there is no requirement to show evidence of a reasonable expectation of success. Further, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In response to appellant's traversal of official notice and well-known statement for claims 7 and 30, Examiner notes the traversal was not timely filed and so therefore is moot. Official notice was taken in the final office action mailed on November 5, 2004. The common knowledge or well-known in the art statement was taken to be admitted prior art because applicant failed to traverse the examiner's assertion of official notice in the response to the final office action filed on March 10, 2005(see MPEP 2144.03 (C)). Despite the fact, references were provided in the advisory action mailed April 3, 2006. Fung(US 5,396,635) discloses a power management unit connected to a bus, i.e. transmit and receive channels(Figure 2, 15; Column 5, Lines 37-45). Gulick(US 6,816,935) discloses a power management unit connected to transmit and receive channels(Figure 1B). Dahlen(US 5,317,749) discloses the use of round robin algorithm for allowing fair use of the shared resource(Column 10, Lines 43-57). Also, Vernon et al.(US 5,088,024) discloses the use of round robin algorithm(Column 4 , Lines 17-45).

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These references are not relied upon in the grounds of rejection but merely to provide evidence in support of the official notice, and therefore are permissible.

In response to appellant's argument that claims 4 and 5 list a long list of registers and that not all registers are shown, Examiner notes that the claims are written in an alternative form. Therefore only one register from the list of registers needs to be shown.

In response to appellant's argument that limitation "at least one of a direct flow control mode and a message flow control to control the flow of data" in claim 16 is not shown by Baker, Examiner notes this claim is written in alternative form. The specification discloses that in the direct flow control mode, a wait state is introduced if a channel or FIFO is disabled, invalid or full (Paragraph 55). Baker discloses a wait state when the channel or FIFO is disabled, invalid or full. Therefore Baker shows direct flow control mode to control the flow of data.

In response to appellant's argument that the limitation of "selecting another one of the plurality of transmit FIFOs to send data to another corresponding one of the plurality of receive FIFOs while the corresponding one of the receive FIFOs cannot receive data" in claim 30 is not shown by Baker, Examiner respectfully disagrees. Baker discloses that several states can occur where the execution of a channel cannot proceed because of a wait state, such as a condition when data cannot be received in the FIFO. Another channel's FIFO can be chosen for execution to proceed if the receive FIFO cannot receive data (Column 14, Lines 20-28; Column 17, Lines 1-15). Therefore Baker discloses the limitation "selecting another one of the plurality of transmit FIFOs to send data to another corresponding one of the plurality of receive FIFOs while the corresponding one of the receive FIFOs cannot receive data."

#### **(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

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For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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